

## CLAIMS

1. An integrated circuit comprising a nonvolatile memory cell comprising:  
  
source/drain regions of a first conductivity type in a semiconductor substrate, and  
a channel region in the substrate between the source/drain regions;  
  
5 a first conductive gate comprising a semiconductor material of a second  
conductivity type opposite to the first conductivity type, the first conductive gate  
overlying a portion of the channel region; and  
  
a floating gate overlying a portion of the channel region.
2. The integrated circuit of Claim 1 wherein the first conductive gate is a gate  
10 of a buried channel transistor.
3. The integrated circuit of Claim 1 wherein the channel region comprises a  
surface region underlying the first conductive gate and having a lower net dopant  
concentration of the second conductivity type than a region immediately below the  
surface region.
- 15 4. The integrated circuit of Claim 3 wherein the surface region is at most  
0.2  $\mu\text{m}$  deep.
5. The integrated circuit of Claim 1 wherein the channel region comprises a  
surface region underlying the first conductive gate and counterdoped with an impurity of  
the first conductivity type.
- 20 6. The integrated circuit of Claim 5 wherein the surface region is at most  
0.2  $\mu\text{m}$  deep.
7. The integrated circuit of Claim 1 wherein the channel region has the  
second conductivity type.
8. The integrated circuit of Claim 1 wherein the first conductive gate is to  
25 turn on the underlying portion of the channel portion to provide access to the memory  
cell.

9. The integrated circuit of Claim 1 wherein the floating gate is one of two floating gates of the memory cell, each floating gate overlying a portion of the channel region.
10. The integrated circuit of Claim 1 wherein the first conductivity type is type N.
11. The integrated circuit of Claim 1 wherein the first conductivity type is type P.
12. An integrated circuit comprising a nonvolatile memory cell comprising:  
source/drain regions of a first conductivity type in a semiconductor substrate, and  
a channel region in the substrate between the source/drain regions;  
a first conductive gate overlying a portion of the channel region; and  
a floating gate overlying a portion of the channel region;  
wherein the first conductive gate is a gate of a buried channel transistor.
13. The integrated circuit of Claim 12 wherein the channel region comprises a surface region underlying the first conductive gate and having a lower net dopant concentration of the second conductivity type than a region immediately below the surface region.
14. The integrated circuit of Claim 13 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.
15. The integrated circuit of Claim 12 wherein the channel region comprises a surface region underlying the first conductive gate and counterdoped with an impurity of the first conductivity type.
16. The integrated circuit of Claim 15 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.
17. The integrated circuit of Claim 12 wherein the channel region has the second conductivity type.

18. The integrated circuit of Claim 12 wherein the first conductive gate is to turn on the underlying portion of the channel portion to provide access to the memory cell.

19. The integrated circuit of Claim 12 wherein the floating gate is one of two floating gates of the memory cell, each floating gate overlying a portion of the channel region.

20. The integrated circuit of Claim 12 wherein the first conductivity type is type N.

21. The integrated circuit of Claim 12 wherein the first conductivity type is type P.

22. A method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions of a first conductivity type in a semiconductor substrate and having a channel region in the substrate between the source/drain regions, the method comprising:

forming a first conductive gate comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and

forming a floating gate overlying a portion of the channel region.

23. The method of Claim 22 wherein the first conductive gate is a gate of a buried channel transistor.

24. The method of Claim 22 wherein the channel region comprises a surface region underlying the first conductive gate and having a lower net dopant concentration of the second conductivity type than a region immediately below the surface region.

25. The method of Claim 24 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.

26. The method of Claim 1 further comprising implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to lie below the first conductive gate.

27. The method of Claim 26 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.
28. The method of Claim 22 wherein the channel region has the second conductivity type.
- 5 29. The method of Claim 22 wherein the first conductive gate is to turn on the underlying portion of the channel portion to provide access to the memory cell.
30. The method of Claim 22 wherein the floating gate is one of two floating gates of the memory cell, each floating gate overlying a portion of the channel region.
31. The method of Claim 22 wherein the first conductivity type is type N.
- 10 32. The method of Claim 22 wherein the first conductivity type is type P.
33. An method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions of a first conductivity type in a semiconductor substrate and having a channel region in the substrate between the source/drain regions, the method comprising:
- 15 forming a first conductive gate overlying a portion of the channel region; and  
forming a floating gate overlying a portion of the channel region;  
wherein the first conductive gate is a gate of a buried channel transistor.
34. The method of Claim 33 wherein the channel region comprises a surface region underlying the first conductive gate and having a lower net dopant concentration
- 20 of the second conductivity type than a region immediately below the surface region.
35. The method of Claim 34 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.
36. The method of Claim 33 further comprising implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface
- 25 region is to lie below the first conductive gate.
37. The method of Claim 36 wherein the surface region is at most 0.2  $\mu\text{m}$  deep.

38. The method of Claim 33 wherein the channel region has the second conductivity type.

39. The method of Claim 33 wherein the first conductive gate is to turn on the underlying portion of the channel portion to provide access to the memory cell.

5 40. The method of Claim 33 wherein the floating gate is one of two floating gates of the memory cell, each floating gate overlying a portion of the channel region.

41. The method of Claim 33 wherein the first conductivity type is type N.

42. The method of Claim 33 wherein the first conductivity type is type P.